DATA SHEET

TDA8041H
Quadrature demodulator controller

Preliminary specification
File under Integrated Circuits, IC03

November 1994

Philips Semiconductors

PHILIPS

Quadrature demodulator controller TDA8041H

FEATURES

- Generates all control signals for Quadrature Phase-Shift Keying (QPSK) and Binary Phase-Shift Keying (BPSK) demodulation
- Can be used in applications with low E_b/N_o and high symbol rate (up to 30×10^6 symbols/s)
- Digital I and Q outputs (3 bits) for soft decision within error correction
- Two matched analog-to-digital converters to quantize the I and Q signals
- A digital detector for each control loop to generate the required control signals
- Digital-to-analog converters and operational amplifiers to allow high flexibility for loop time constants
- Special input stage to interface with the voltage controlled crystal oscillator
- Positive 5 V supply voltage.

APPLICATIONS

- Demodulation of BPSK and QPSK modulated signals in satellite and telephone applications.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		4.75	5.0	5.25	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		4.75	5.0	5.25	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		4.75	5.0	5.25	V
V_{DDD}	supply voltage for digital section (pin 35)		4.75	5.0	5.25	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		4.75	5.0	5.25	V
$I_{DD(tot)}$	total supply current	V_{DD} = 5 V	–	30	–	mA
V_{IQ}	I and Q input voltage		–	1.0	–	V
R_{sym}	symbol rate		–	–	30×10^6	symbols/s
$I_{O(DAC)}$	DAC output current		−100	–	+100	mA

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA8041H	QFP44[1]	plastic quad flat package; 44 leads (lead length 1.3 mm); body $10 \times 10 \times 1.75$ mm; high stand-off height	SOT307-2

Note

1. When using reflow soldering it is recommended that the Drypack instructions in the *"Quality Reference Handbook"* (order number 9398 510 63011) are followed.

BLOCK DIAGRAM

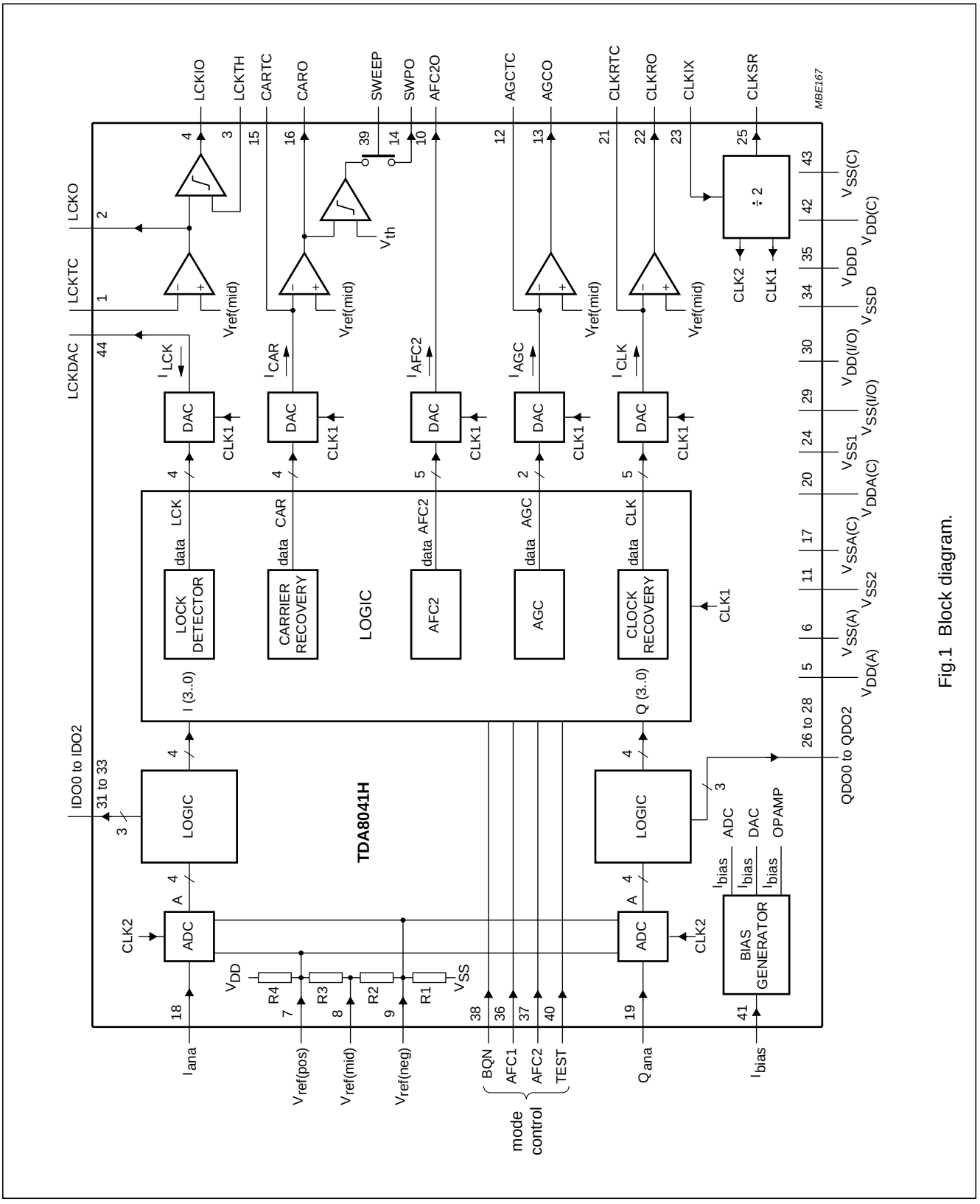


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
LCKTC	1	carrier lock time constant
LCKO	2	carrier lock output
LCKTH	3	carrier lock threshold voltage
LCKIO	4	carrier lock indicator output
$V_{DD(A)}$	5	supply voltage for operational amplifiers
$V_{SS(A)}$	6	negative supply voltage for operational amplifiers
$V_{ref(pos)}$	7	positive reference voltage for converters
$V_{ref(mid)}$	8	middle reference voltage for converters
$V_{ref(neg)}$	9	negative reference voltage for converters
AFC2O	10	AFC 2 output
V_{SS2}	11	negative supply voltage 2
AGCTC	12	automatic gain control time constant
AGCO	13	automatic gain control output
SWPO	14	sweep current output
CARTC	15	carrier recovery time constant
CARO	16	carrier recovery output
$V_{SSA(C)}$	17	analog negative supply voltage for converters
I_{ana}	18	analog input I
Q_{ana}	19	analog input Q
$V_{DDA(C)}$	20	analog supply voltage for converters
CLKRTC	21	clock recovery time constant
CLKRO	22	clock recovery output
CLKIX	23	clock input from crystal circuit (at double symbol rate)

SYMBOL	PIN	DESCRIPTION
V_{SS1}	24	negative supply voltage 1
CLKSR	25	clock output at symbol rate
QDO2	26	Q digital output (bit 2)
QDO1	27	Q digital output (bit 1)
QDO0	28	Q digital output (bit 0)
$V_{SS(I/O)}$	29	negative supply voltage for digital inputs/outputs
$V_{DD(I/O)}$	30	supply voltage for digital inputs/outputs
IDO2	31	I digital output (bit 2)
IDO1	32	I digital output (bit 1)
IDO0	33	I digital output (bit 0)
V_{SSD}	34	negative supply voltage for digital section
V_{DDD}	35	supply voltage for digital section
AFC1	36	AFC control switch 1 (1 = on; 0 = off)
AFC2	37	AFC control switch 2 (1 = on; 0 = off)
BQN	38	BPSK/QPSK control switch (1 = BPSK; 0 = QPSK)
SWEEP	39	sweep control switch (1 = on; 0 = off)
TEST	40	test control switch (1 = on; 0 = off)
I_{bias}	41	input bias current for analog blocks
$V_{DD(C)}$	42	supply voltage for digital part of ADC and DAC
$V_{SS(C)}$	43	negative supply voltage for digital part of ADC and DAC
LCKDAC	44	carrier lock DAC output

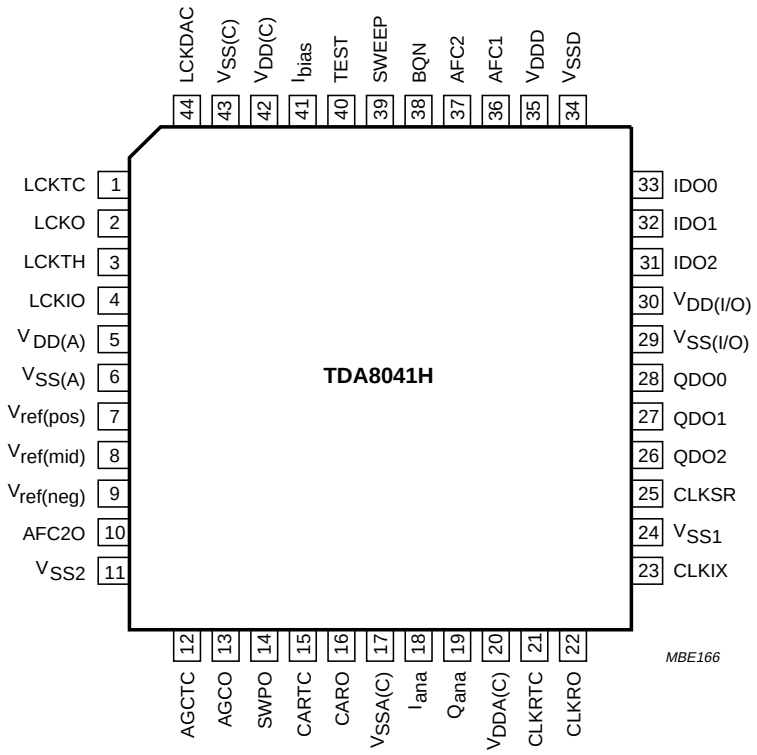


Fig.2 Pin configuration.

GENERAL DESCRIPTION

The quadrature demodulator controller TDA8041H, generates all control signals required for demodulation of BPSK and QPSK modulated signals. This device is specially designed to be used in conjunction with the quadrature demodulator IC, TDA8040T.

The quadrature demodulator controller generates the following signals:

- Symbol clock recovery control signal; this signal locks the VCXO to the received symbol clock. The clock recovery algorithm used in this device operates independently from the other loops.
- Carrier recovery control signal; depending on the selected mode (BPSK or QPSK), this signal will adjust the phase of the I and Q input signal. This adjustment will be such that the constellation points are as defined in Fig.4.
- Frequency control signals (AFC1 and AFC2); to serve a broad range of applications, two different AFC detectors and a sweep function are built-in:
  - AFC1: this is a robust detector which forces the offset frequency in the I and Q branch to zero. This detector can handle frequency offset up to 1/8 × symbol rate.
  - AFC2: this detector can handle frequency offsets greater than 1/8 × symbol frequency. However this AFC algorithm will bring the offset frequency only close to zero.
  - Sweep: this signal generates a triangular current output which can tune a VCO over its complete frequency range. Sweeping must be switched off as soon as the logical output of the lock detect function becomes positive. The value of the sweep current is set by an external resistor.
- Amplitude control signals (AGC); this signal adjusts a variable gain amplifier so that the amplitude of the I and Q signals is in accordance with the specified constellation points of Fig.4.
- Lock detect signal; this signal is related to the E_b/N_o of the incoming I and Q signals. This lock detect signal can be used for two purposes:
  - Lock detection by comparing the lock detect signal with an external set reference voltage, one can obtain a logical signal indicating lock detect.
  - The relationship between E_b/N_o can be used to display the E_b/N_o for antenna adjustment.

FUNCTIONAL DESCRIPTION

The TDA8041H has a 3-bit-wide digital I and Q output for soft error correction. These 3-bit outputs represent the main symbols only. The relationship between the 4-bits ADC signals and the 3-bit output signals is illustrated in Fig.3.

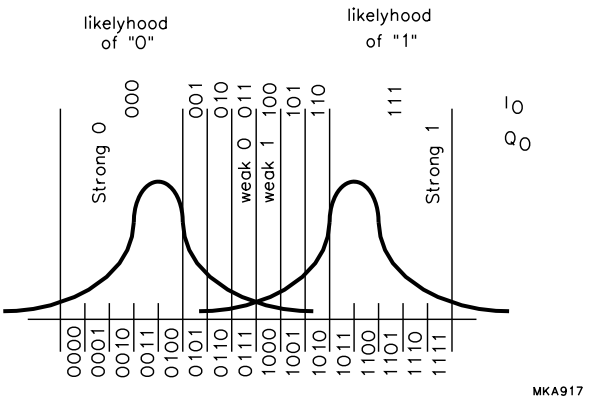


Fig.3 I and Q output levels for soft error decision FEC.

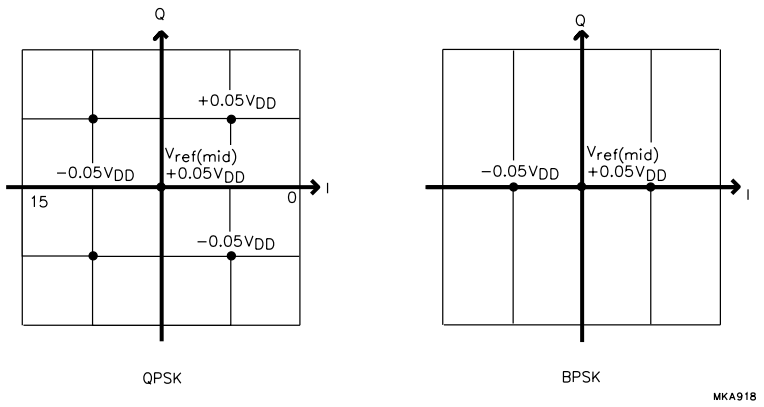


Fig.4 Constellation points.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DD(A)}$	supply voltage for operational amplifiers (pin 5)		–0.5	+6.5	V
$V_{DDA(C)}$	analog supply voltage for converters (pin 20)		–0.5	+6.5	V
$V_{DD(I/O)}$	supply voltage for digital inputs/outputs (pin 30)		–0.5	+6.5	V
V_{DDD}	supply voltage for digital section (pin 35)		–0.5	+6.5	V
$V_{DD(C)}$	supply voltage for digital part of ADC and DAC (pin 42)		–0.5	+6.5	V
$V_{n(max)}$	maximum voltage on all pins		0	V_{DD}	V
P_{tot}	total power dissipation	T_{amb} = 70 °C	–	500	mW
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–	+150	°C
T_{amb}	operating ambient temperature		0	+70	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	75	K/W

HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, to be totally safe, it is desirable to take normal precautions appropriate to handling MOS devices.

CHARACTERISTICS

V_{DD} = 4.75 to 5.25 V; $R_{sym} = 30 \times 10^6$ symbols/s; T_{amb} = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Digital outputs (pins 26 to 28 and 31 to 33)						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage	see Fig.6	$0.9V_{DD}$	–	V_{DD}	V
t_d	delay time	see Fig.6	t_h	–	22	ns
t_h	hold time		8	–	t_d	ns
Digital inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
C_I	input capacitance		–	–	10	pF
Clock output (pins 22 and 25); see Fig.5						
V_{OL}	LOW level output voltage		0	–	$0.1V_{DD}$	V
V_{OH}	HIGH level output voltage		$0.9V_{DD}$	–	V_{DD}	V
T_{cy}	cycle time		33	–	–	ns
t_W	pulse width	duty cycle 40/60	13.2	–	–	ns
t_r	rise time	C_L = 30 pF	–	–	6	ns
t_f	fall time	C_L = 30 pF	–	–	6	ns
Clock input (pin 23)						
R_{source}	source resistance		–	–	50	Ω
f_s	sampling frequency		–	–	60	MHz
Analog inputs (pins 18 and 19)						
R_{sym}	symbol rate		–	–	30×10^6	symbols/s
$V_{ref(pos)}$	positive reference voltage	I_O = 0	–	$0.48V_{DD}$	–	V
$V_{ref(mid)}$	middle reference voltage	I_O = 0	–	$0.38V_{DD}$	–	V
$V_{ref(neg)}$	negative reference voltage	I_O = 0	–	$0.28V_{DD}$	–	V
I_L	load current at pin 8	note 1	–5	–	+5	mA
$V_{i(I,Q)}$	I and Q input voltage		0	–	V_{DD}	V
$V_{I,Q(op)}$	I and Q operating voltage		$0.28V_{DD}$	–	$0.48V_{DD}$	V
R_I	input resistance		50	–	–	kΩ
C_I	input capacitance		–	–	20	pF
I_{bias}	input bias current	R_L = 100 kΩ	–	–37	–	mA
DAC outputs (pins 10, 12, 15 and 21)						
$I_{o(av)}$	average output current	$V_{DAC} = V_{ref(mid)}$; note 2	–	100	–	mA
D_{Io}	matching of positive and negative output currents	$V_{DAC} = V_{ref(mid)}$; note 2	–7	–	+7	%
I_o	zero output current		–25	–	+25	nA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Sweep current (pin 14)						
V_{OH}	HIGH level output voltage		–	$2V_{ref(mid)}$	–	V
V_{OL}	LOW level output voltage		–	0	–	V
Z_O	output impedance	SWEEP = 1	–	2	–	kΩ
		SWEEP = 0	10	–	–	MΩ
$V_{CARO(min)}$	LOW switching level		$0.1V_{DD}$	–	$0.2V_{DD}$	V
$V_{CARO(max)}$	HIGH switching level		$0.8V_{DD}$	–	$0.9V_{DD}$	V
Loop amplifiers						
V_o	output voltage		$0.1V_{DD}$	–	$0.9V_{DD}$	V
G_v	open loop gain		–.	60	–	dB
G_B	gain bandwidth		–	1	–	MHz
R_L	load resistance		5	–	–	kΩ

Notes

1. $V_{ref(mid)}$ is usually open-circuit. However, this pin may also be used as a reference output for an external buffer.

2. $I_{o(av)} = \frac{(I_{pos} - I_{neg})}{2}$; $D_{Io} = 100 \times \frac{(I_{pos} + I_{neg})}{(I_{pos} - I_{neg})}$

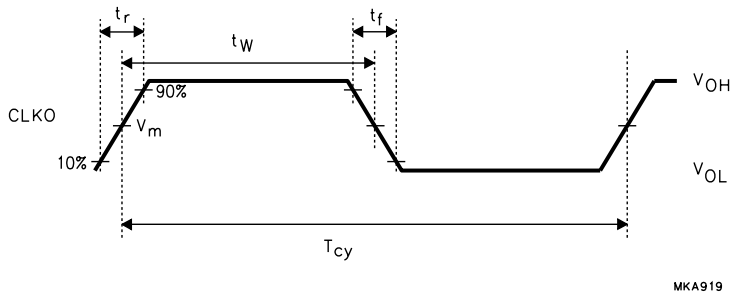


Fig.5 Timing of CLKO.

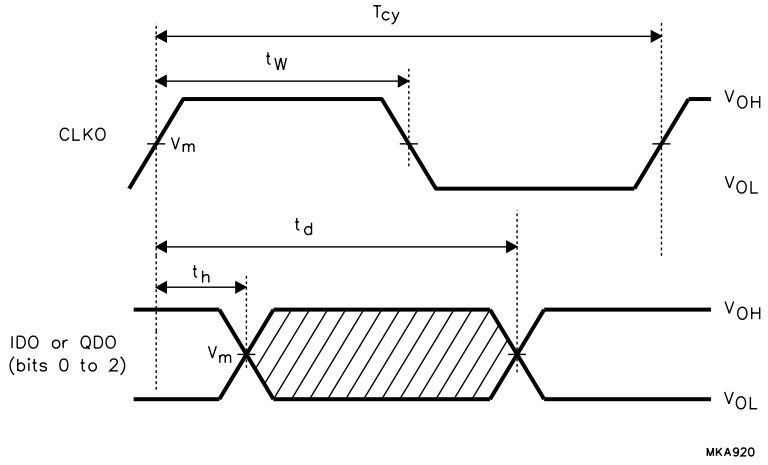


Fig.6 Timing definition of digital outputs.

APPLICATION INFORMATION

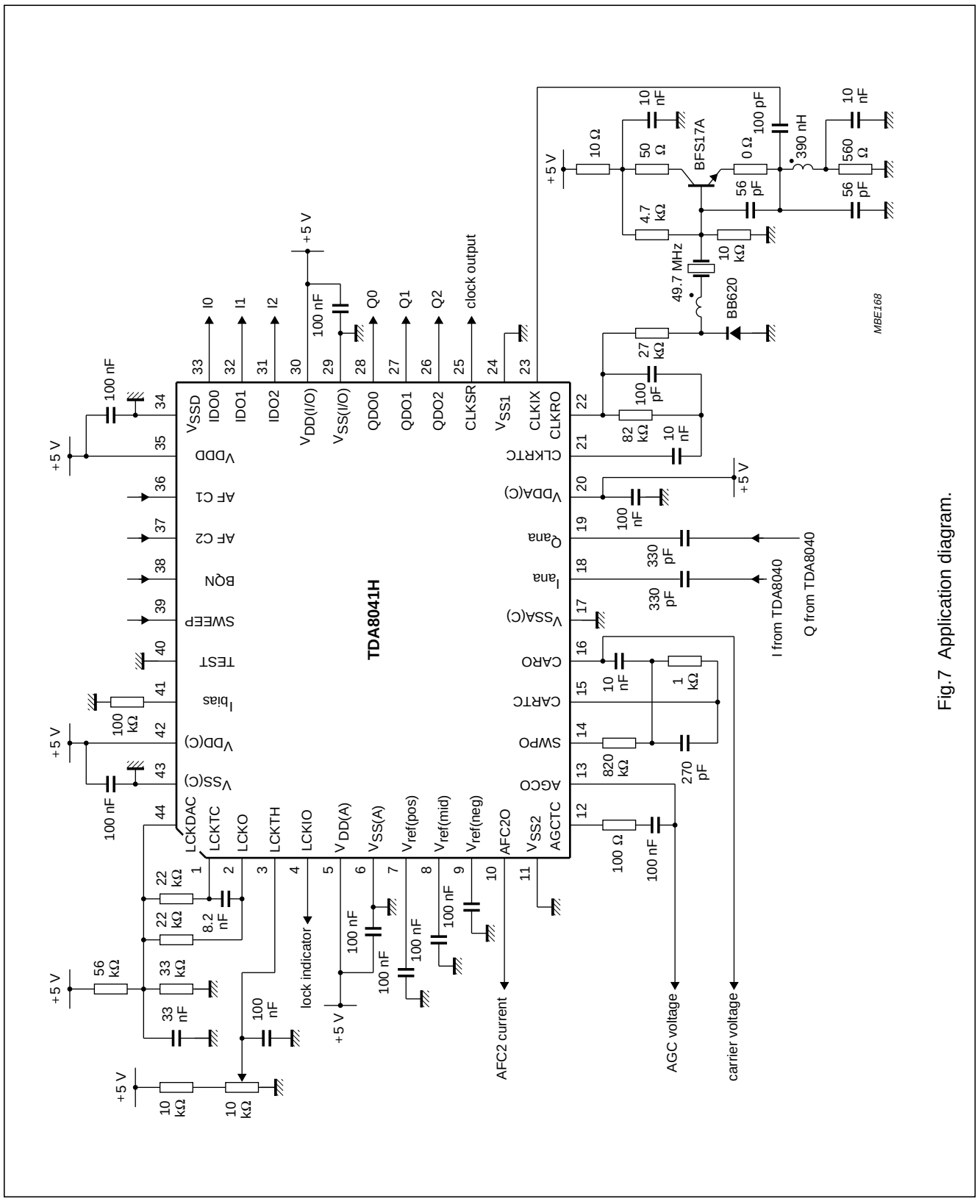
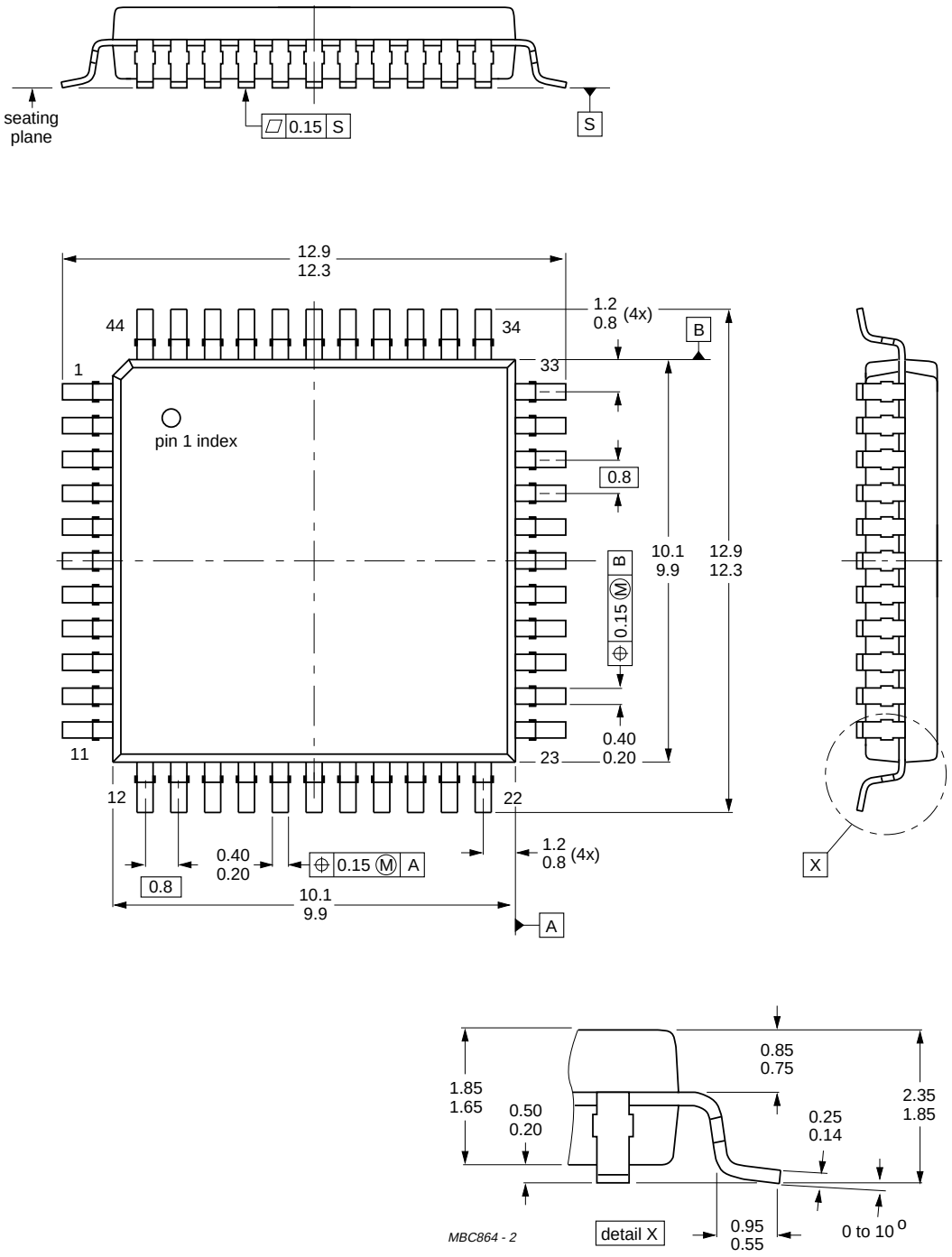


Fig.7 Application diagram.

PACKAGE OUTLINE



Dimensions in mm.

Fig.8 Plastic quad flat package; 44 leads (lead length 1.3 mm); body 10 × 10 × 1.75 mm; high stand-off height (QFP44; SOT307-1).

SOLDERING

Plastic quad flat-packs

BY WAVE

During placement and before soldering, the component must be fixed with a droplet of adhesive. After curing the adhesive, the component can be soldered. The adhesive can be applied by screen printing, pin transfer or syringe dispensing.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder bath is 10 s, if allowed to cool to less than 150 °C within 6 s. Typical dwell time is 4 s at 250 °C.

A modified wave soldering technique is recommended using two solder waves (dual-wave), in which a turbulent wave with high upward pressure is followed by a smooth laminar wave. Using a mildly-activated flux eliminates the need for removal of corrosive residues in most applications.

BY SOLDER PASTE REFLOW

Reflow soldering requires the solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the substrate by screen printing, stencilling or pressure-syringe dispensing before device placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt, infrared, and vapour-phase reflow. Dwell times vary between 50 and 300 s according to method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 min at 45 °C.

REPAIRING SOLDERED JOINTS (BY HAND-HELD SOLDERING IRON OR PULSE-HEATED SOLDER TOOL)

Fix the component by first soldering two, diagonally opposite, end pins. Apply the heating tool to the flat part of the pin only. Contact time must be limited to 10 s at up to 300 °C. When using proper tools, all other pins can be soldered in one operation within 2 to 5 s at between 270 and 320 °C. (Pulse-heated soldering is not recommended for SO packages.)

For pulse-heated solder tool (resistance) soldering of VSO packages, solder is applied to the substrate by dipping or by an extra thick tin/lead plating before package placement.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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NOTES

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